PHASE LOCKED LOOP INCLUDING CONTROL CIRCUIT FOR REDUCING LOCK-TIME

Abstract of the Disclosure

A PLL circuit includes a control circuit for generating a reference control signal. A reception divider, reference divider, and transmission divider respectively divide an output signal of a receiver VCO according to a reception division data signal, an output signal of a crystal oscillator according to a reference division data signal, and an output signal of a transmitter VCO according to a transmission division data signal. A first and second phase detector respectively detect frequency and phase differences between a reception divider output and a reference divider output and between a transmission divider output and the reference divider output.